Radiation Evaluation of the 80C186 1 6-B t Microprocessor Utilizing an In-Circuit Emulator for In-Situ Electrical Biasing and Characterization

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Abstract

Radiation characterization data for the 80C1 86 I 6-bit microprocessor for two manufacturers are presented. An approach using an in-circuit cmulator (ICE) to implement in-situ dynamic biasing and functional testing was used. Test results showed parametric failure levels I hat differ by more than afactor of 1 () between devices from two manufacturers. Accelerated annealing meas urement s show that the Intel mi croprocessor dots not anneal significantly until the annealing temperature is elevated to 150 °C while the Advanced Micro Devices (AMD) device exhibits more rapid annealing, characteristics. Implications for space application and hardness assurance are discussed.

Introduction

The 80C 186 is a CMOS high-integrationmicroprocessor. Features include a 1) RAM refresh control unit, power-save mode, programmable interrupt controller, programmable memory and peripheral chip select logic, and two independent DMA channels. The Intel80C186 microprocessor is manufactured on a 1.5 µm CHMOS process line. This microprocessor was originally introduced in 1992, and it is the second generalion of what is nowalarge family of X86CPU's that includes the Pentium® family of processors.

The 80C 186 has been used in spacecraft applications for many years [1]. It is the most critical part of electronic systems and is used in applications where the microprocessor is controlling communication, altitude control and otherhousekeeping duties of lilt spacecraft. Because of the 80C 186's low cost and mature developmental tool and programming base, it continues to be a microprocessor of choice for many space applications.

Previous tests have shown that the radiation failure level of other members of the Intel CPU family is approximately 15 krad(Si) [2-8]. Typically, existing total dose radiation test data is based on simplified testing approaches (such as static bias or simple clocking arrangements) that do not fully exercise the microprocessor. More comprehensive microprocessor tests with functional tests involve complicated test setups that are extremely costly and time consuming [2-12].

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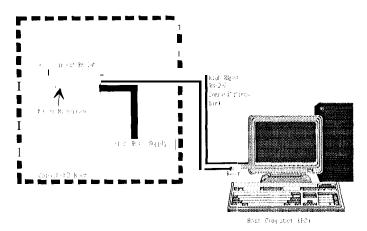
Another limitation of conventional microprocessor testing approaches is the expensive and time consuming development of test vector sets to perform functional characterization tests on an automatic test equipment. 1 n the current environment of highly constrained budgets and limited resources, it is important to explor c anti-develop new, low cost methods of generating radiation test data. In this paper, we introduce a low cost method for a functional test by generating test vector sequences for insitu-dynamic operation and electrical characterization of a microprocessor utilizing an ICE.

Using an ICE to operate a microprocessor during total dose radiation allows the test engineer a much wider degree of freedom and control over the microprocessor under test than more conventional methods. The ICE gives a user nearly complete control over the operation of the microprocessor allowing the user to bias and exercise a very complicated circuit in a precise, cost effective manner, This approach could easily be utilized on more advanced microprocessors such as: 80C386, 80C486 and Pentium as ICEs are currently available for those microprocessors.

Experimental Approach

A "[)(1) mom type gamma source (Shepherd Model 8 i) was used for all radiation exposures, Al i devices were irradiated using a lead aluminum equilibrium shield. Calibration was performed using MDH Ilonchambers with accuracy traceable to NIST. Dose rates used for this series of tests ranged from 1() to '25 rad(S1)/s,

A block diagram of the basic setup for the radiation biasing scheme used in this work is shown in Figure 1. The ICE and associated hardware used for this test cost less than \$5,000, A special 900 turn socket was fabricated so that ICE electronics could be shielded more effectively while allowing the microprocessor to be in the line of sight of the radiation source. With the ability to place the ICE scar the radiation source, a capability is developed whereby considerable control over the microprocessor under test is available for in-situ testing. This approach allowed the microprocessor to run almost any code necessary to test all modules and units of the device under test by using a remote computer over an 1{ S-232 high-speed serial link. Any register may be interrogated, traced and controlled. Virtually



I figure I. Basic setup diagram of an ICE test approach.

any sequence of codes can be executed, including, flight codes. A drawback of this approach is that once the microprocessor fails functionally, the ICE becomes inoperable because, the ICE uses the microprocessor under test as the system controller. Note, however, that some ICEs are designed with two microprocessors. This allows the DUT to be a second device and therefore avoid the aforementioned drawback.

TestVehicles

1 ntel devices were from a military wafer lot t hat were in fact the actual space flight lot. These devices were manufactured to military specifications with the exception of radiation tolerance. Incidentally, Intel no longer manufactures the 8(K186 microprocessors, All Intel devices were from a die bank. However, AM I> continues to make the 80C186 and all AM I> devices used for this test were fabricated with a commercial CMOS process. Intel devices were packaged in accramic quad flat pack (CQFP), while AMD devices were in plastic leaded chip carriers (PLCC).

Electrical Biases

Two electrical biases were used during radiation: Static and dynamic. Static bias was achieved through the use of specially fabricated cards that held all inputs and outputs of the device either at the power supply voltage (5.0 V) or ground, in-situ dynamic biasing consisted of running, a sieve program, written in C, which locales prime numbers. Devices remained biased at all times during, and after irradiation except for short t imes during measurement.

Measurement and Irradiation Sequencing

1 Data were taken on the WC186 microprocessors from the Intel and AMD using the test sequence that follows. Electrical characterization tests were performed on a Hewlett-Packard 82000 digital test system, while the ICE was used to test functionality. A typical test sequence was executed as follows:

I) Perform electrical measurement tests using the HP82000.

- 2) Perform functional test using the ICE.
- 3) Place DUT into place for irradiation.
- 4) Initialize the functional test code and irradiate the DUT.
- 5) Monitor the functionality of the DUT during irradiation.
- 6) Alter irradiation, perform functional tests with the ICE.
- 7) Perform post electrical tests using HP82000. Repeatsteps3through7 until the device exhibits failure or until the highest radiation level desired is achieved.

Test Results

The most sensitive.smralnetets were standby current (Istatic) and operating supply current (Iop) during irradiation. These currents were also the most critical parameters in the actual applications because, the system power module could only provide limited power to the microprocessor. Electrical measurements were taken at the following frequencies: Static, 10 MHz, 12 MHz and 16 MHz. Figure 2 shows the results for the Intel and AM D microprocessors. The dose rate was 10 rad(Si)/s and all devices were dynamically biased during irradiation.

There is a large difference in radiation performance between the Intel and AMI) processors, The AMI) device exhibits a more gradual degradation than does the Intel device. Although the AM 1) microprocessor was still functional in the ICE at 1 00 krad(Si), the supply current exceeded over 200 mA at 16 MHz. The maximum AMID specification limit of dynamic supply current at 16 MHz is 80 mA and was first exceeded at 30 krad(Si). The 1 ntel microprocessor exceeded the maximum specification limit of 160 mA at 10 krad(Si). Dynamic supply current at 12 MHz reached a maximum of well over 500 mA at 14 krad(Si) where the functional failure was observed. Mechanisms for each type of behavior will be discussed later in the paper.

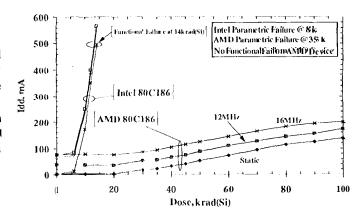


Figure 2. Power supply current measured at several frequencies verses dose for the AMD and Intel microprocessors. Note the large difference in radiation response between the two microprocessors.

Post irradiation annealing tests were performed for devices shown in Figure 2. This consisted of dynamically biased room temperature anneals for 144 hours for Intel devices and 20 hours for AMD devices. Dynamic bias was achieved using the ICE with the same program running as during the irradiation test. Both devices recovered partially but not fully. Annealing data will be discussed in the next section of this paper.

Accelerated Annealing Test Results

Several accelerated anneal sequence tests were performed for this experiment. Intel devices were subjected to long term statically biased isothermal anneals. The anneal temperatures used were 25, 60, 100, and 150 °C. Figure 3 plots the supply current at 12 MHz as a function of time for the above temperatures. Note that no significant annealing occurred except at the anneal temperatures of 100 and 150 °C. At the 100 °C anneal temperature, supply current recovers to within about 25% of preirradiation values after 2000 hours. The 150 °C anneal showed complete recovery within 300 hours.

To further investigate annealing in the 80C186, an isochronal anneal test was performed on an Intel device. Figure 4 shows the results of this annealing test on the supply current for several operating frequencies. The isochronal annealing test was performed by placing a statically biased sample into an oven and elevating the temperature to the needed level for a period of one hour. Devices were then removed from the oven and left under bias and allowed to cool for electrical measurements. After measurements were made, the sample was then returned to the oven and heated to the next higher anneal temperature. In Figure 4, note that significant annealing does not occur until a temperature of 160 °C is reached. At 200 °C almost all of the radiation damage has been annealed out.

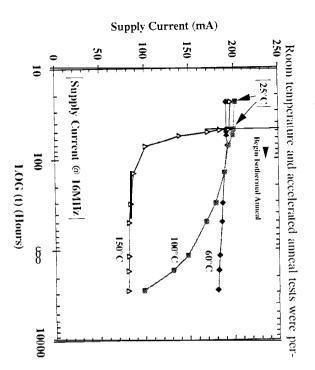


Figure 3. Isothermal annealing data for the Intel 80C186 using supply current at 16MHz. Note that annealing is completed at 300 hours @ 150°C.

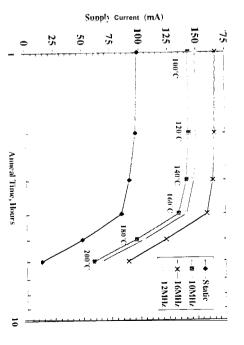


Figure 4. Isochronal annealing data for the Intel 80C186. Note that significant annealing does not take place until annealing temperature reaches 160°C.

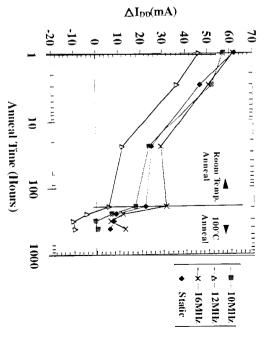


Figure 5. Post radiation and accelerated annealing data for the AMD 80C186. Note that relative to the Intel device, this device anneals very rapidly. Recovery is almost complete within 24 hours at 25°C.

formed on the AMD microprocessor as well. Figure 5 shows the supply current at several operating frequencies versus time. Note that supply current anneals rapidly compared to the Intel microprocessor. By the 24 hour post radiation measurement supply current in the AMD device has recovered to within 10-30% of pre-radiation values at room temperature, whereas temperatures above 100 °C were required to anneal damage in the Intel device. This type of behavior causes in the AMD device to be more sensitive to dose rate than the Intel device. Implications for hardness assurance will discussed in a later section of the paper.

Discussion

Differences in Radiation Response

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Differences in failure mode between Intel and AMD devices could be explained by a number of mechanisms. However, the large difference in performance in the AMD and Intelmicroprocessors improbably due to gate and field oxide leakage mechanisms. The Intel device, with a rapid increase in supply current followed by functional failure indicates field oxide leakage mechanism. The current increased very rapidly at about 8 krad(Si), and functional failure is likely due to the large leakage current from field oxide inversion. On the other hand, the AMD device exhibited a slower, more gradual increase in supply current, indicating a gate oxide leakage mechanism [13].

In addition to the pronounced difference in supply current degradation, the ICE approach showed that the AMD devices would operate functionally at levels of 100° krad(Si). This was more than one order of magnitude higher than the functional failure level of the Intel devices. Tests with the ICE at different clink rates showed that clock frequency had little effect. On radiation degradation. Tests with different instruction sets also bad little effect On the functional Or parametric failure level.

Implications for Space Applications

There are several implications for space application resulting Irwin this wink. First, for the Intel 80C186, applying the actual low dose rate in the space, environment will not improve the radiation performance of the classic because the damage is stable for long time periods. Annealing test results showed that temperatures in excess of 140 °C were required to cause significant annealing. It is very important to note that the radiation test data in Figure 2 for the Intel device is close to what may be expected in a typical space application.

The AMD device appears to be a better choice for space applications, al least from a total dosc irradiation perspective. With total dosc hardness almost a factor Of ten greater than the Intel device, and favorable annealing characteristics, the AMD microprocessor should perform to higher total dosc levels when irradiated at space dose rates (< 0.01 rad(Si)/s). Other reliability issues need to be addressed before the AMD device can be used in a space flight applications, First, tile single event latchup (SEL) and SEU threshold must be determined for this device. Packaging is an another issue as the AMD product is currently available only in plastic packages, and it is unclear that AMD will manufacture any parts to meet military class electrical performance characteristics and specifications.

Overall, the test results in this paper indicate the extreme importance Of doing radiation lot acceptance testing on all commercial devices, even if the process has shown to be historically radiation tolerant. Total dose lot acceptance testing needs to be performed even though a commercial product is being

manufactured to military specifications as that is no indication of radiation performance

Summary

lonizing radiation data on the AMD and Intel 80C18616-bit microprocessorhas been completed using a cost effective ICE testing approach. Radiation response between manufacturers was shown to differ by more than a factor of ten. Annealing test results were presented which showed that the Intel device elms not anneal significantly until anneal temperature was elevated to 150 °C AMD devices exhibited more rapid annealing and as such were much more responsive to dose rate than the Intel devices. In addition, the functional failure levels of the AMD (it)' iccs\~c[-c{ JI~c(~l(iel of magnitude greater than that of devices from Intel. Isothermal and Isochronal anneal data were presented for Intel devices.

References

- [1] A. Holmes-Siedle and L. Adams, <u>Handbook Of Radiation Effects</u>. First Edition, (Oxford, Oxford University Press, p. 143, 1993).
- [2] S. Yoshioka et al, "A Radiation-Hardened 32 bit Microprocessor Based on the Commercial Process," IEEE Trans. Nucl. Sci., NS-412481-2486, 1994.
- [3] S. G.Mulford, "TotalDoseRadiation Testing of the Intel 80386DX Microprocessor and 80387DX Math Coprocessor Using a Personal Computer Motherboard for the Test Fixture," IEEE <u>NSREC Workshop Record</u>, 26-29, 1994.
- [4]A. K. Sharma, K. Sahu and J. 1 ander, "An f (valuation of the Radiation Tolerance of a 32-bit Microprocessor for Space Applications," IEEE NSREC Workshop Record, 30-36, 1994.
- [5] A.H. Johnston, "Annealing of Total Dose Damage in the Z80 Microprocessor," IEEE Trans. Nucl. Sci., NS-30, 4251, 1983.
- 6]E.W Sexton et. al, "Radiation Testing of the CMOS 8085 Microprocessor Family," IEEE Trans Nucl. Sci., NS-30, 4253, 1983.
- [7]R.Kogaet.al, "Techniques of Microprocessor Festingand SEU-Rate Predictions," IEEE Trans. Nucl. Sci., NS-32, 4219, 1985.
- [8] K.J. Hass et. al, "A Radiation Hardened 16/32-bit Microprocessor," IEEE Trans. Nucl. Sci., <u>NS</u>-36, 2252-2257, 1989.
- [9] J.H. Elder, J. Osborn, W.A. Kolasinski, R. Koga, "A Method For Characterizing a Microprocessor's Vulnerability to SEU," IEEE Trans. Nucl. Sci., NS-35, 1678-1681, (1988).
- [10] B.L. Gingerich, J.M. Hermsen, J.C. Lee, "Total Dose Rate Radi at ion Characterization of f.PI-CMOS Radiation f ardned Memory and Microprocessor Devices," IEEE Trans. Nucl. Sci., NS-31, 1332-1336, (1984).
- [1]] K. Marks and P. Measel, "Total Dose Test Results for the 8086 Microprocessor," IEEE Trans. Nucl. Sci., NS-29, 1662-1664, (1982).
- [12] F.W. Sexton et. al, "Radiation Testing of the 8085 Microprocessor Family," IEEE Trans. Nucl Sci., NS-30, 4235-4239, (1983).
- [13] T.P Ma anti P.V. Dressendorfer, Ionizing Radiation Effects in MOS Devices and Circuits, First Edition, (New York, Wiley, p.179, 1989.